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	Filing Date		2006-07-19	
	First Named Inventor	Dasu, Aravind R.		
	Art Unit	2193		
	Examiner Name	Bullock, Jr., Lewis Alexander		
Attorney Docket Number		117316-155055		

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1	Fredriksson, Kimmo "Faster String Matching with Super-Alphabets" Proc of SPIRE' 2002, Lecture Notes in Computer Science 2476, pages 44-57, Springer Verlag, Berlin 2002	<input type="checkbox"/>
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12	Iseli, C. et al. "A C++ Compiler for FPGA Custom Execution Units Synthesis" IEEE Symposium on FPGAs for Custom Computing Machines, 1995	<input type="checkbox"/>
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23	Kuramochi, M., et al. "An Efficient Algorithm for Discovering Frequent Subgraphs" Technical Report 02-026, University of Minnesota, 2002	<input type="checkbox"/>
24	Kwok, Y.K., et al. "Dynamic Critical-Path Scheduling: An Effective Technique for Allocating Task Graphs to Multiprocessors" IEEE Transactions on Parallel and Distributed Systems, Vol. 7, NO 5, May 1996 pp. 506-521	<input type="checkbox"/>
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28	Li, S., et al. "Configuration Code Generation and Optimizations for Heterogeneous Reconfigurable DSPs" Proceedings of SIP99	<input type="checkbox"/>
29	Li, W., et al. "Routability Prediction for Hierarchical FPGAs" Ninth Great Lakes Symposium on VLSI, pp. 256-259, 4-6 March 1999	<input type="checkbox"/>
30	Liu, J. et al. "Variable Instruction Set Architecture and Its Compiler Support" IEEE Transactions on Computers, 2003	<input type="checkbox"/>
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33	Messmer, B.T., et al. "A decision tree approach to graph and subgraph isomorphism detection" Pattern Recognition, 32: 1979-1996, 1999	<input type="checkbox"/>

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34	Mirsky, E. et al. " MATRIX: A Reconfigurable Computing Architecture with Configurable Instruction Distribution and Deployable Resources" IEEE Symposium on FPGAs for Custom Computing Machines, April 17-19, 1996, Napa, CA	<input type="checkbox"/>
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45	Rewini, H., et al. "Static Scheduling of Conditional Branches in Parallel Programs" Journal of Parallel and Distributed Computing, 24, 4154 (1995)	<input type="checkbox"/>
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49	Schoner, B., et al. "Issues in Wireless Video Coding using Run-Time-reconfigurable FPGAs" Proc of the IEEE Symposium on FPGAs for Custom Computing Machines, Napa CA, April 19-21, 1995	<input type="checkbox"/>
50	Singh, A., et al. "Efficient circuit Clustering for Area and Power Reduction in FPGAs" ACM Transactions on Design Automation of Electronic Systems, Volume 7, Issue 4, October 2002, pp. 643-663	<input type="checkbox"/>

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